Single photon processing at high rate with pixel detectors from particle physics

Erik H.M. HEIJNE

CERN EP Division

WORKSHOP on
DETECTORS for
SYNCHROTRON RESEARCH

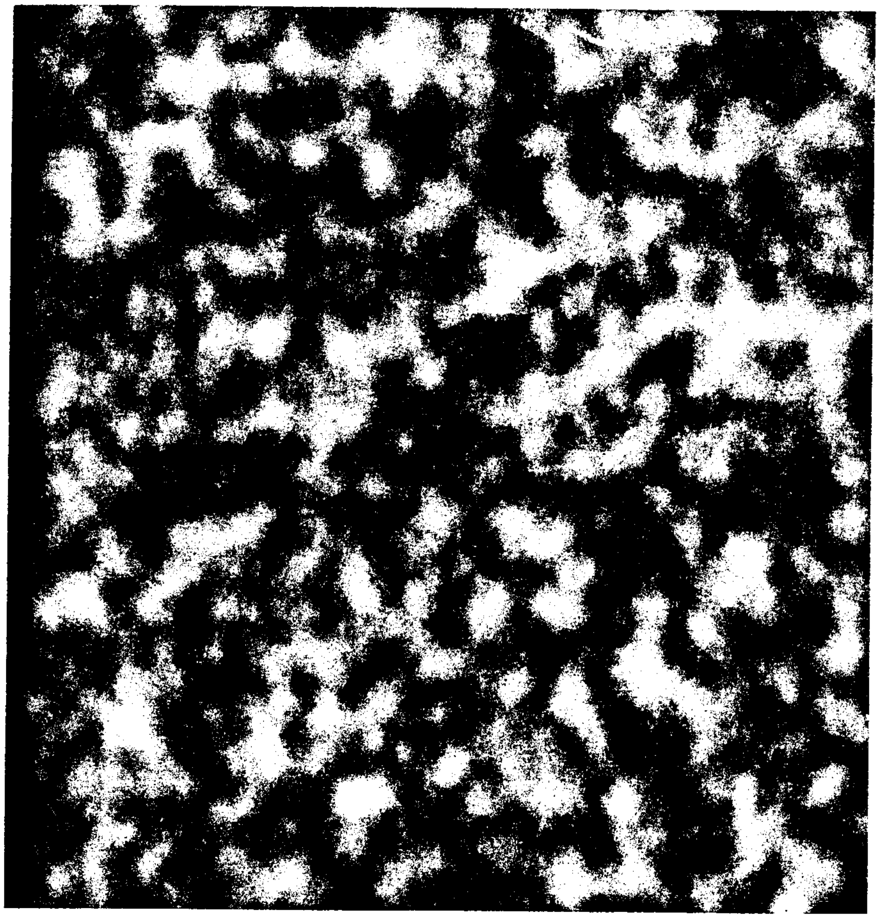
WASHINGTON

30-31 Oct 2000

CONTENTS

FIXED TARGET EXPERIMENT
HEAVY-ION EVENT

Pb ion in OMEGA spectrometer



RD19

WA97

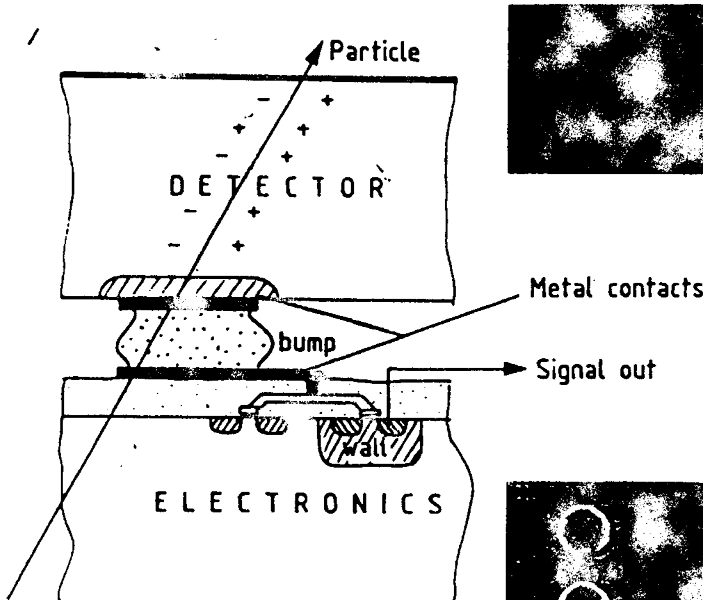
TRACKING using PIXEL DETECTOR TELESCOPE

Erik HEIJNE

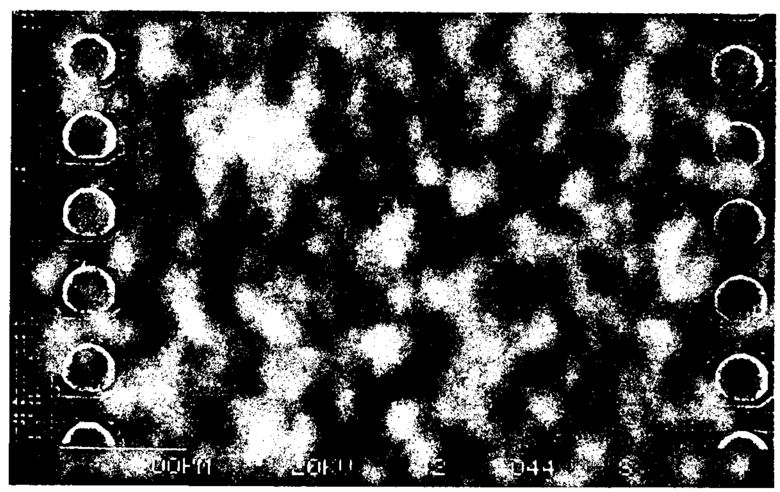
CERN EP - Div

PIXELS in PARTICLE PHYSICS
HYBRID Si SENSOR

SENSOR M
Si



BUMPS



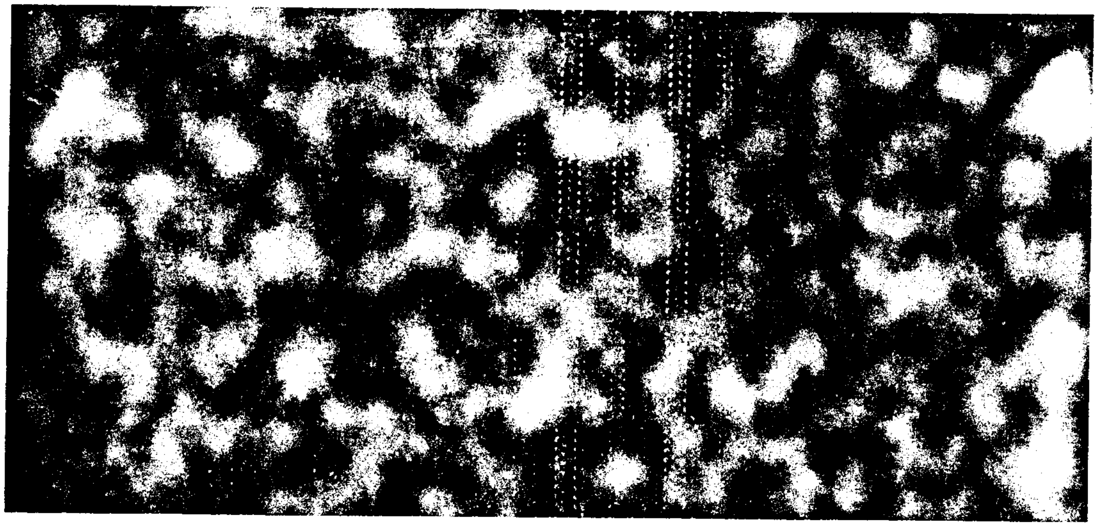
READOUT ELECTRONICS

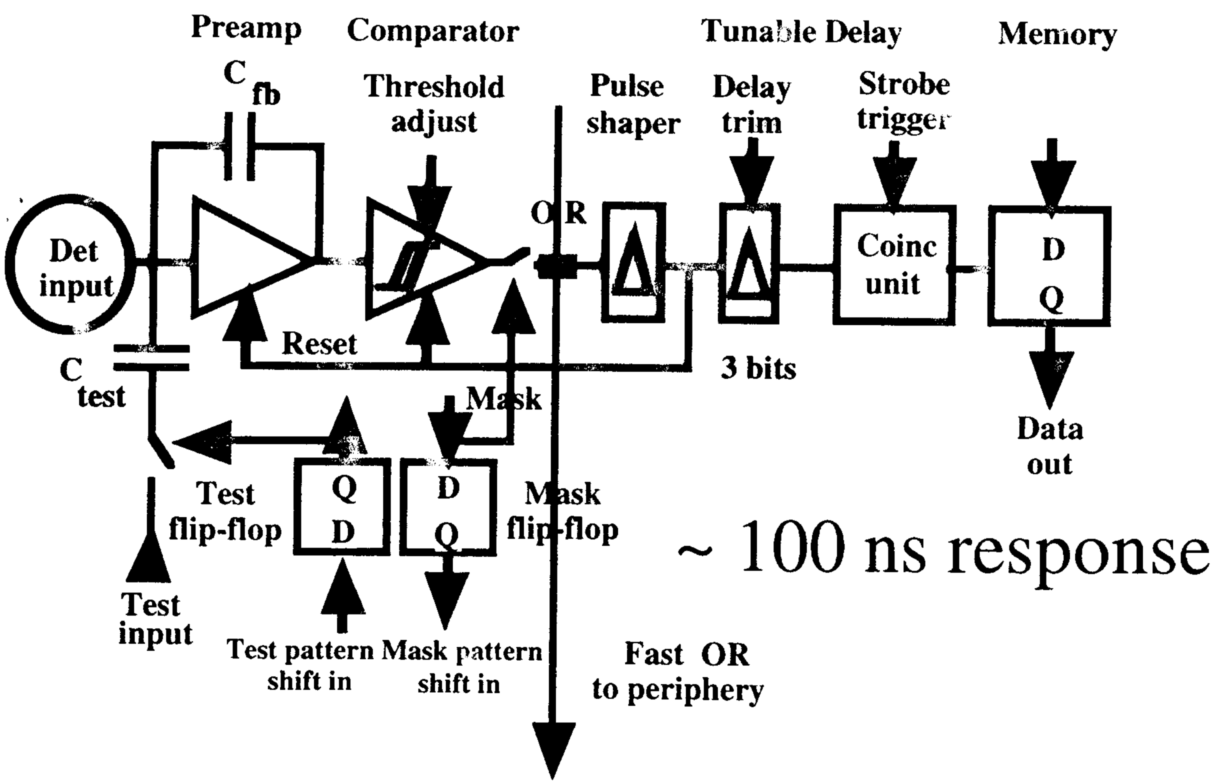
Erik HEIJNE

CERN EP - Div

PIXELS in PARTICLE PHYSICS
Chips at CERN

LHC1 PIXEL READOUT **50μm x 500μm**





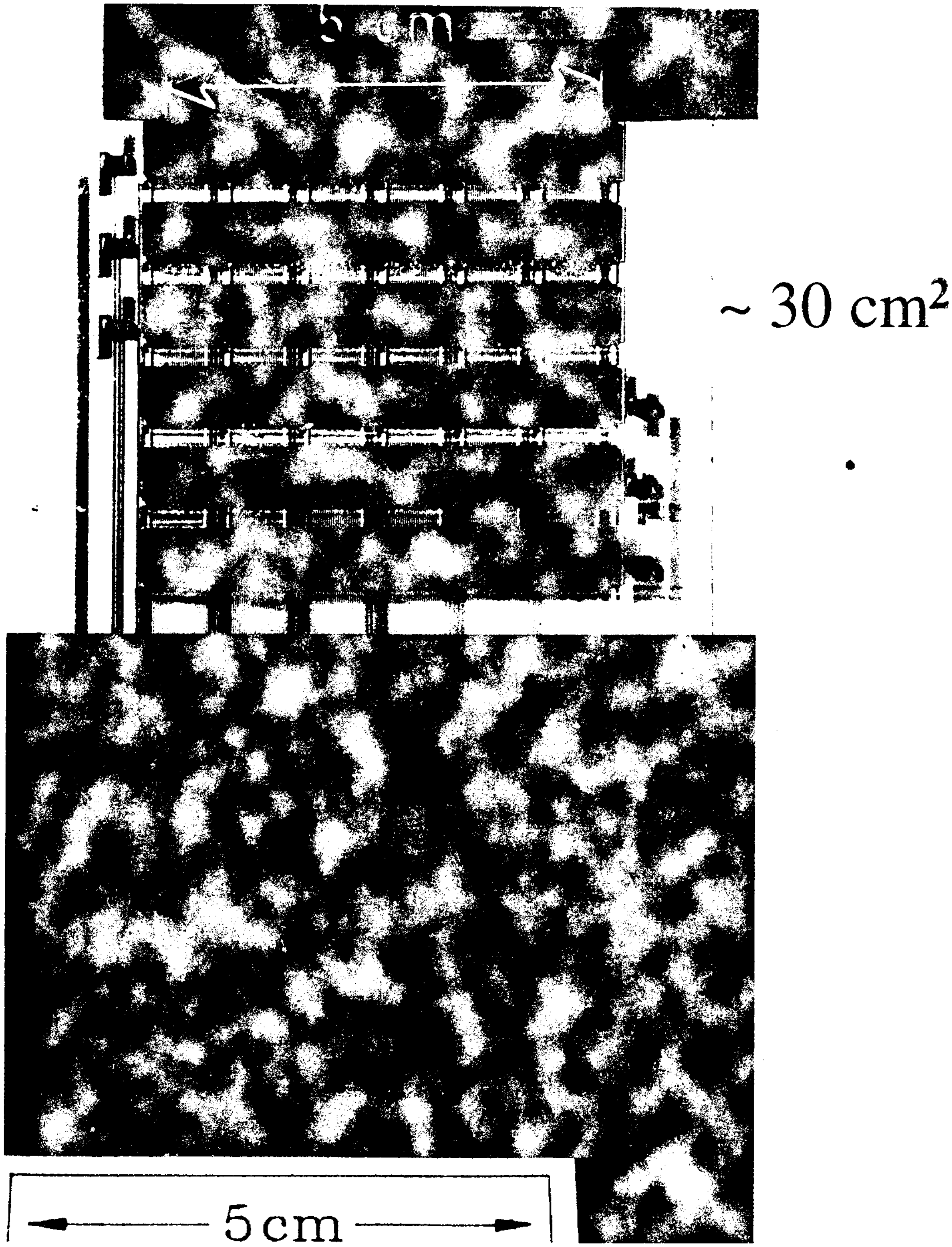
ELECTRONICS DIAGRAM SINGLE PIXEL

Erik HEIJNE

CERN EP - Div

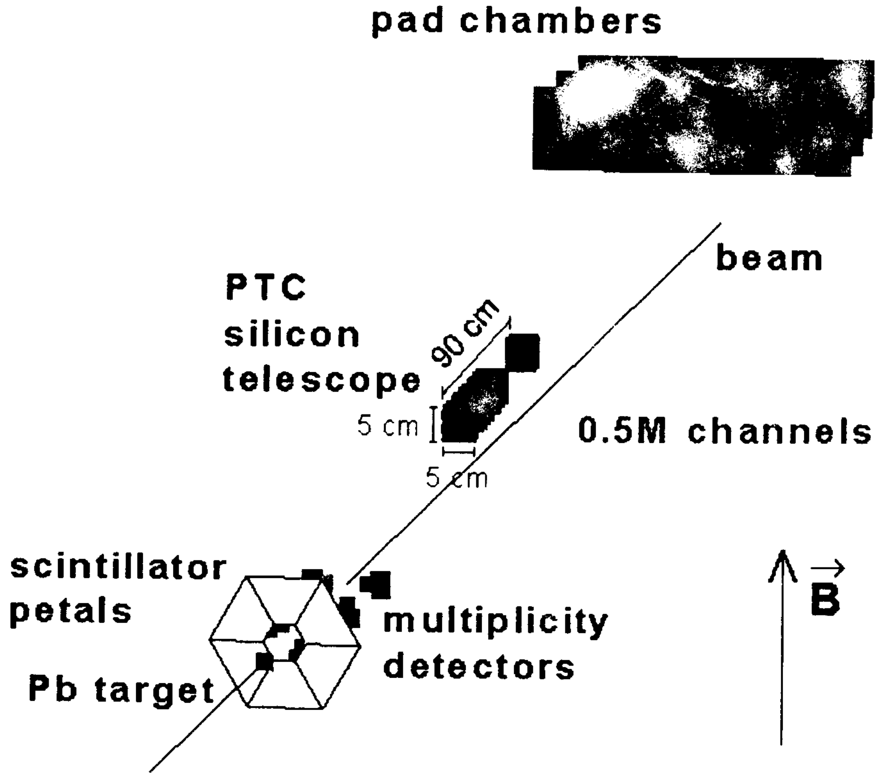
'REACTIVE' PIXELS at CERN

ARRAY of 6 LADDERS, 36 CHIPS



VIEW of LADDERS and CHIPS

WA97 set-up
in the Omega magnet



PIXEL TELESCOPE

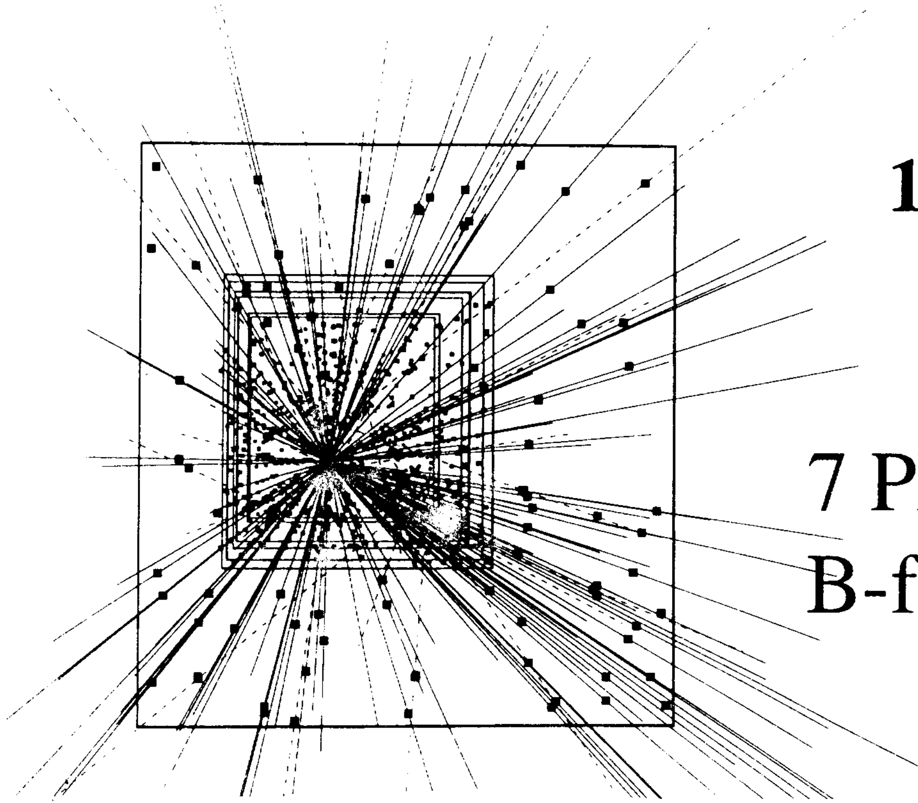
CHIPS -> LADDERS ->

ARRAYS -> PLANES

4, 7, 14 PLANES IN USE

TRACKING with PIXELS at CERN

WA97 RD19



153 tracks

7 PLANES
B-field OFF

^{208}Pb ion at 158 GeVA on Pb target

Millions of EVENTS ANALYZED

SPACE POINTS
NOISE-FREE

PIXELS in PARTICLE PHYSICS
2 SYSTEMS at CERN

WA97-NA57 HEAVY-ION EXP

14 PLANES USED, 800 CHIPS, 400 cm^2

1994 - now

DELPHI e - p COLLIDER EXP

4 CROWNS, 2500 CHIPS, 1400 cm^2

1997 - now

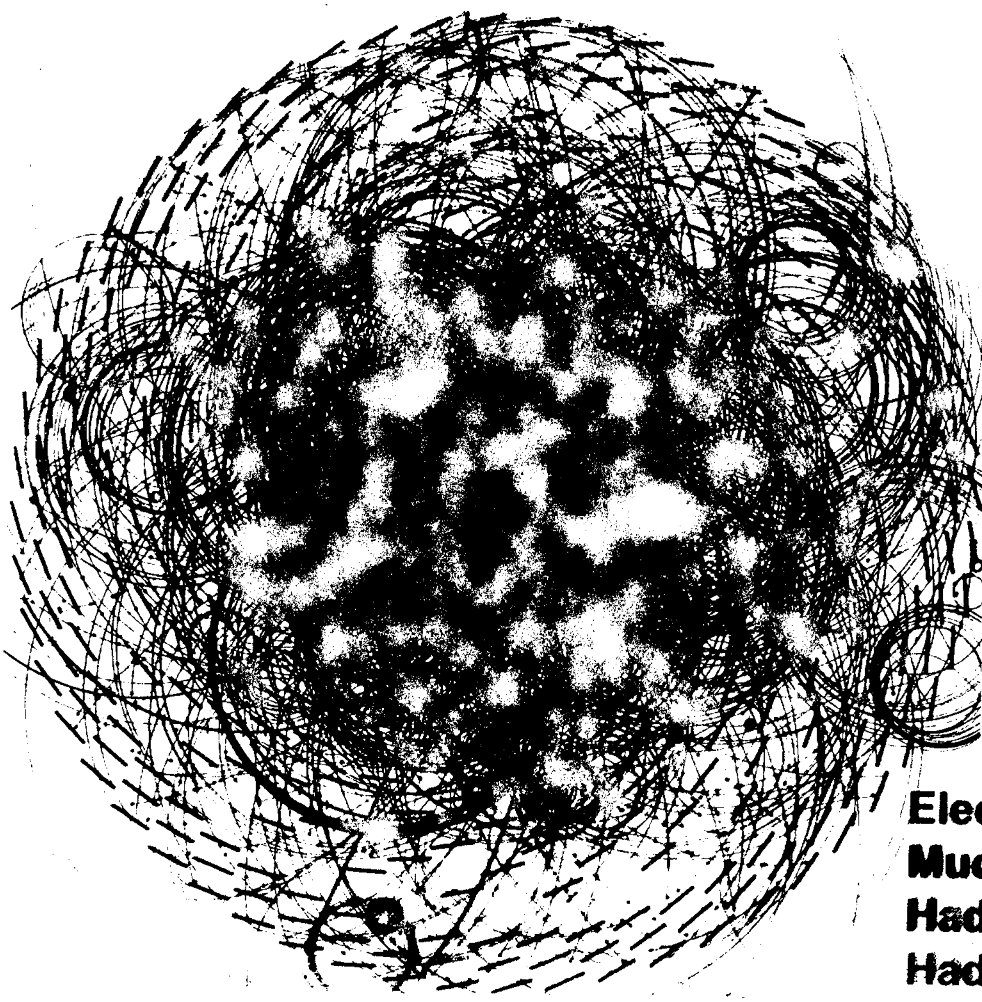
several LHC EXPTS planned

FUTURE PARTICLE PHYSICS EXPERIMENTS at CERN

HEAVY-ION & COLLIDER expts

HIGH MULTIPLICITY several 100s

HIGH RATE 40 MHz



CMS

H ->μμμμ

m(H)=150GeV

+ 20 Min bias

1m

Electrons

Muons

Hadrons pt<2GeV

Hadrons pt>2GeV

HIGHLY SEGMENTED, FAST, RADHARD DETECTORS NEEDED

SIGNAL in 100 μm Si : 8000 e^- ~ 30 keV

Erik HEIJNE

CERN EP - Div

ISSUES in TRACKING

2-D SEGMENTATION in PIXELS

SPACE POINTS ~ 10 μm

LOW CAPACITANCE <100 fF

-> NOISE 50 - 150 e^- rms

-> THIN SENSOR 80 μm ?

-> SPEED signal < 10 ns

HIGH MULTIPLICITY

coincident particles

BINARY or ANALOG READOUT

INTERP OLATION

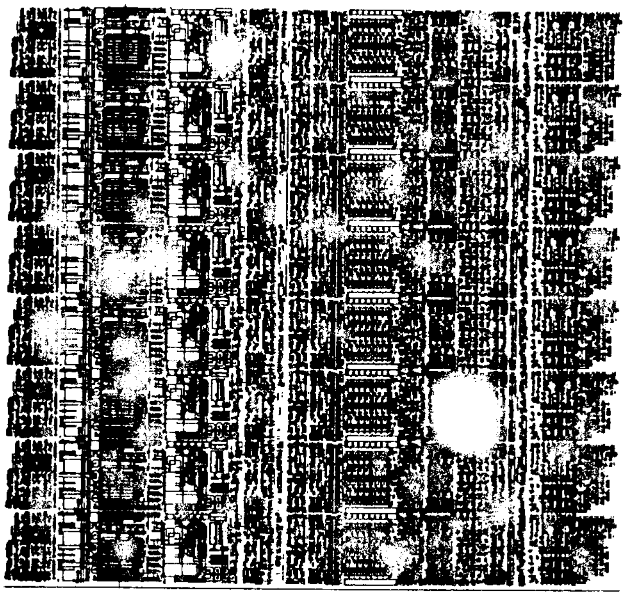
THRESHOLD SETTING

ALIGNMENT of MODULES

PIXELS easier than 1-D projection

FUTURE PIXEL DETECTORS in PARTICLE PHYSICS

eg ALICE HEAVY-ION EXP

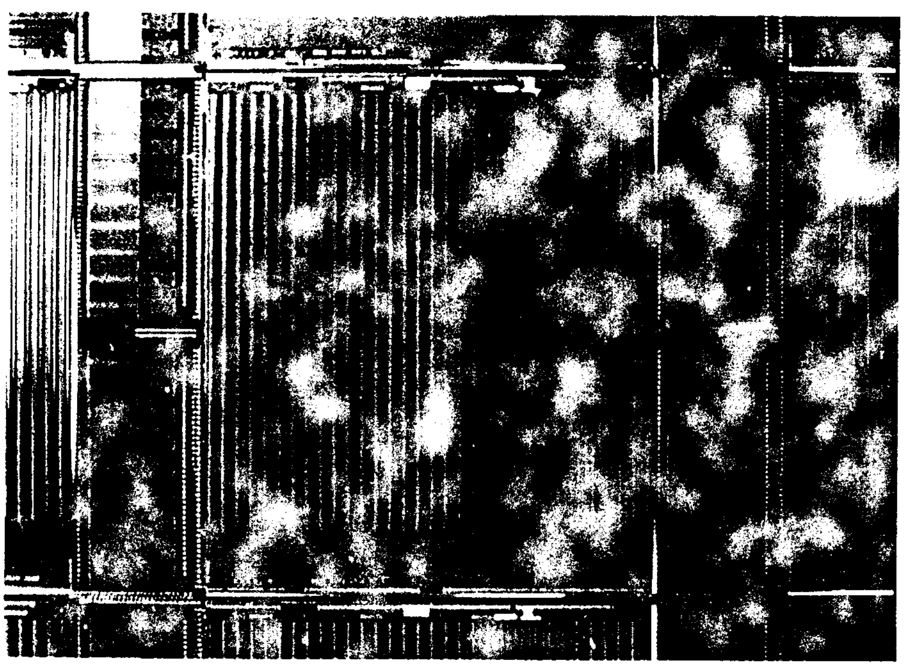


8 cells, blocked

radhard 30 Mrad

400μm x 425μm

8000 pixels, 13 M transistors, 2.2 cm^2



COMPLEXITY in PIXEL

CMOS can be used for ANALOG

DENSITY

LOW POWER

LOW NOISE

SIGNAL PROCESSING on

SINGLE QUANTA

CONTACTS with NEIGHBOURS

COMPENSATE for

SENSOR IMPERFECTIONS

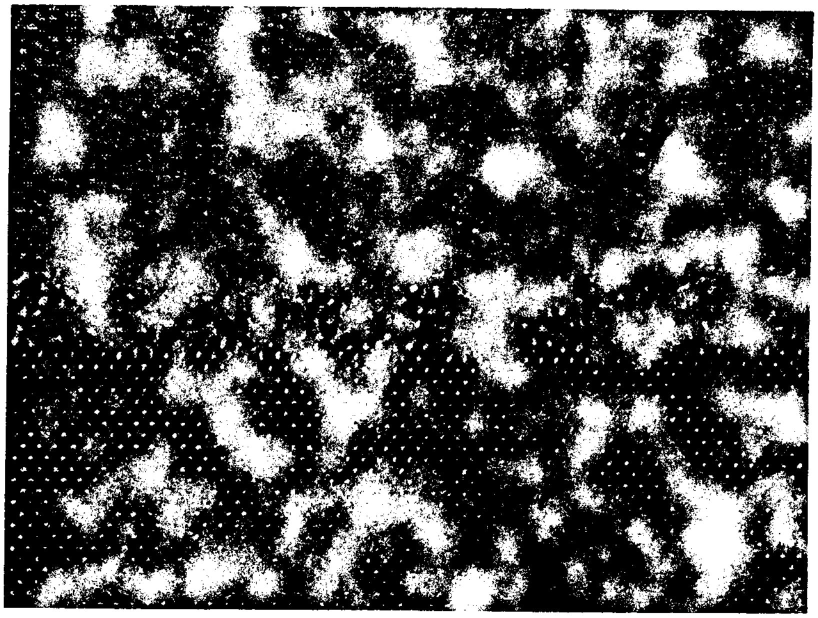
TRIMMING GAIN, THRESHOLD

SYSTEM TEST, CONTROL

INTEGRATE ANCILLARY FUNCTIONS

Impact of Deep-submicron CMOS

MOS Gate TEM Bell Labs April 2000



Poly Si

SiO_2 **1.6 nm**

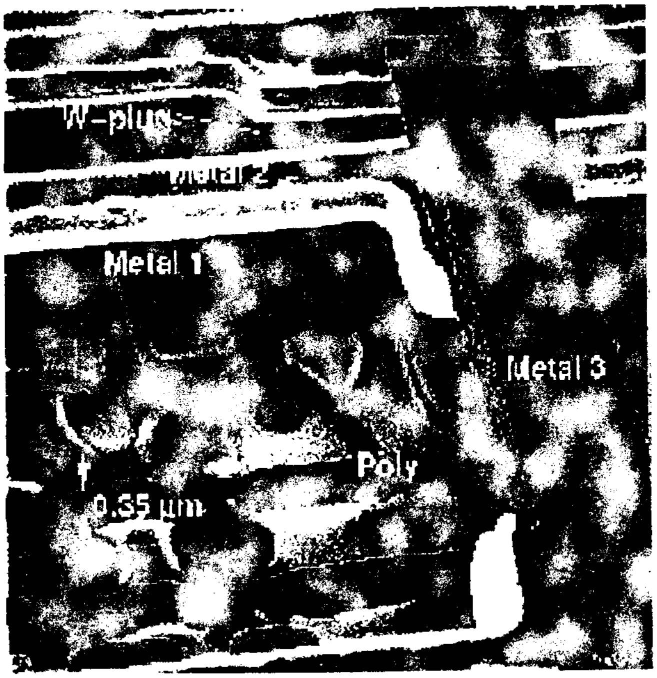
Si

Reliable oxides can be made with only ~ 6 atoms in SiO_2 layer

SiO_2 CMOS technology used down to ~ 0.08 μm transistors

Thin gate oxide (< 8 nm) also is unaffected by radiation (test > 30 Mrad)

PIXEL readout relies on Deep-submicron CMOS



Lucent Technologies
Bell Labs Innovations

poly Si gate

length .35 µm

3 metals shown

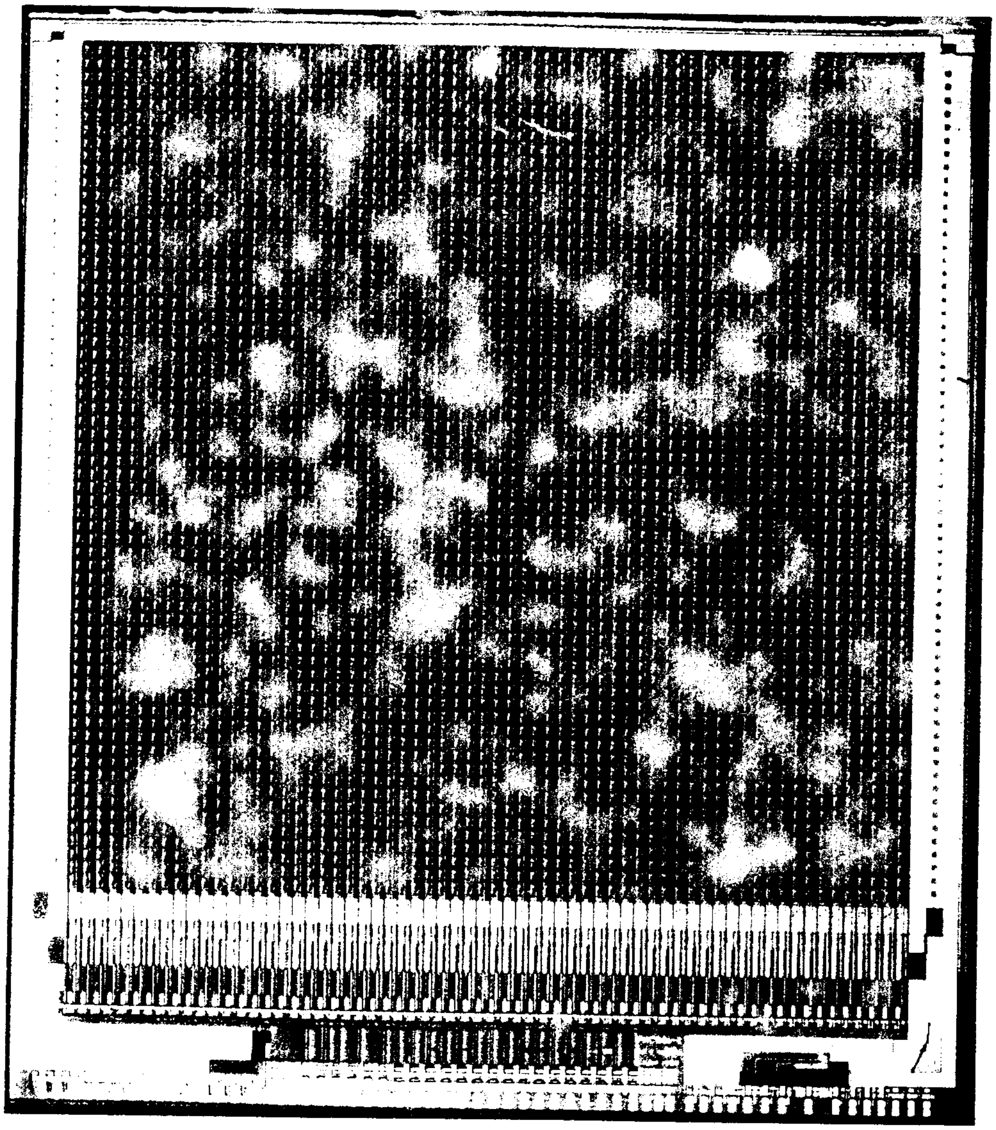
Component density +
6 to 9 levels of interconnect

Pixel chips at CERN now 0.25 µm

FUNCTIONS SPEED
LOW NOISE LOW POWER

Photon Counting Chip CERN

PCC1 64 x 64 PIXELS 170μm x 170 μm



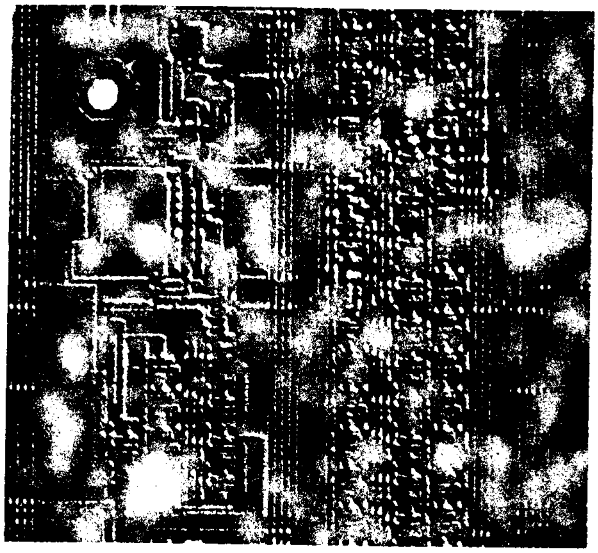
1997

Amplifier-Shaper **1 μm SACMOS**
Comparator 3-bit adjust
16 bit counter common electronic shutter
Dark current compensation per column 10 nA
Readout 384 μs

Erik HEIJNE

CERN EP - Div

Photon Counting Chip CERN



170µm x 170 µm

15 - bit COUNTER

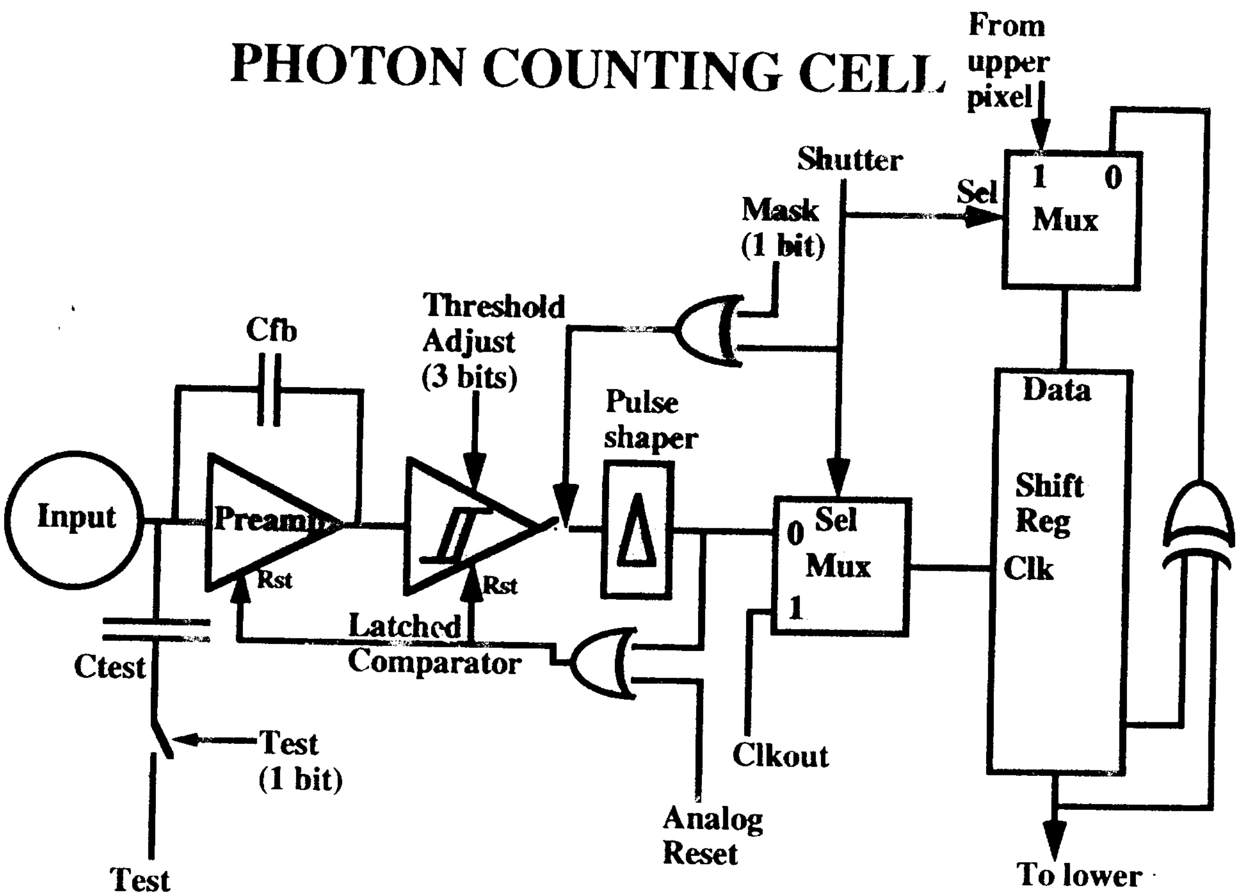
STATIC LOGIC

400 transistors

Bumpbonding

Si or GaAs sensor

PHOTON COUNTING CELL



THRESHOL D ADJUST using 3 bit TRIM

Photon Counting Chip CERN
SUMMARY

150 ns **PEAKING TIME** (rate < 5 MHz)

HIGH COUNT RATE

~ 10^9 $s^{-1}cm^{-2}$

Maximum occupancy ~ 50%

ELECTRONIC NOISE ~170 e^- rms

DARK CURRENT COMPENSATION

10 nA / pixel

30 μA cm^{-2}

TEST SIGNAL INDIVIDUAL PIXELS

MASKING of BAD PIXELS

THRESHOLD ADJUSTABLE

~120 e^- rms

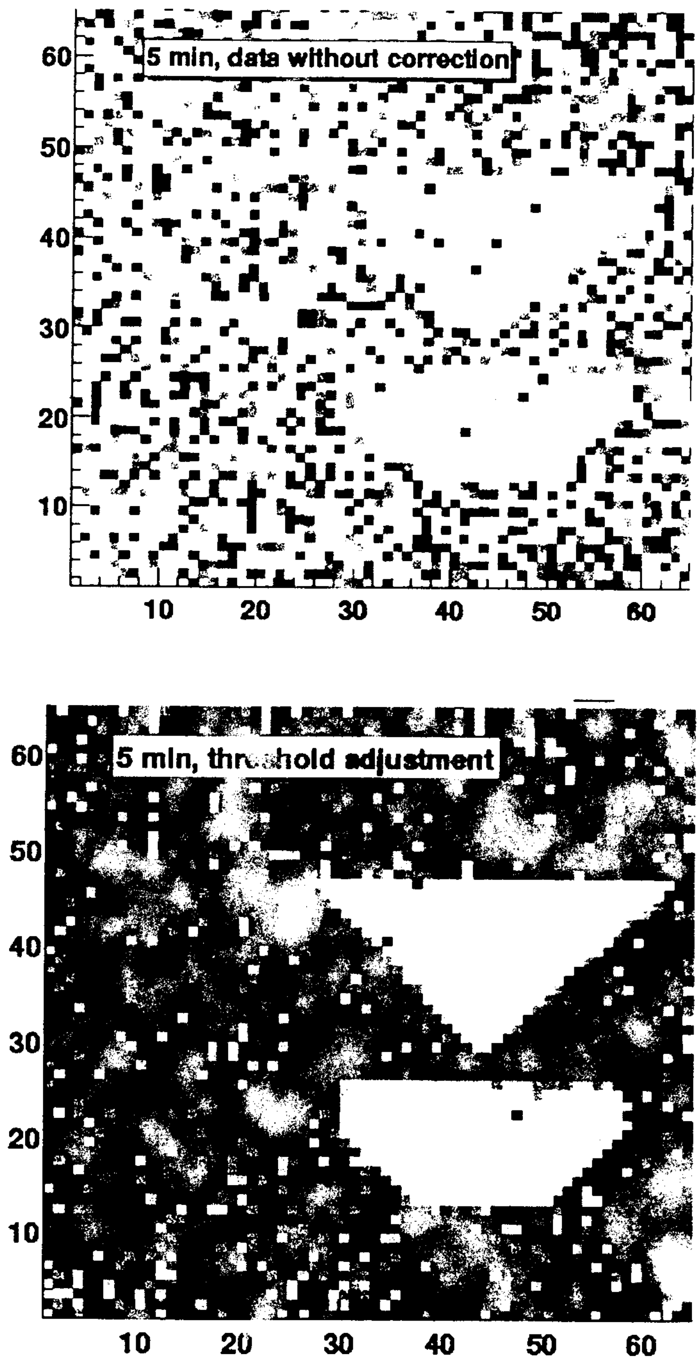
ALLOWS LOW THRESHOLD

~1400 e^- 5 keV

READOUT TIME 384 μs per CHIP

Photon Counting Chip CERN

EFFECT OF THRESHOLD ADJUST



NO ADJUST

WITH

2 PIECES of 100 µm THICK Si : SOURCE ^{55}Fe

Erik HEIJNE

CERN EP - Div

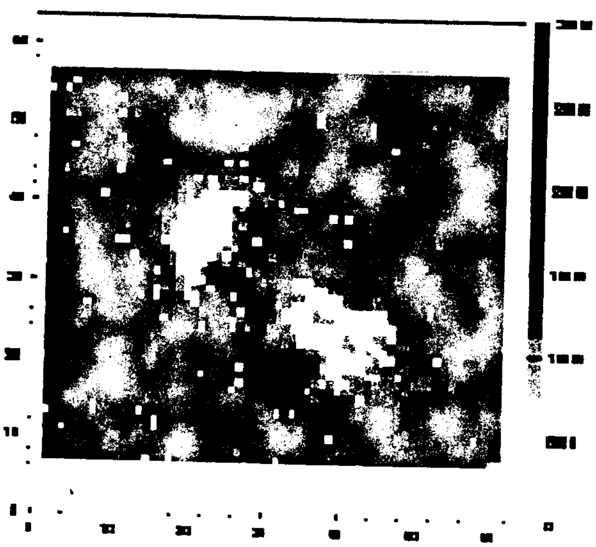
Photon Counting Chip CERN

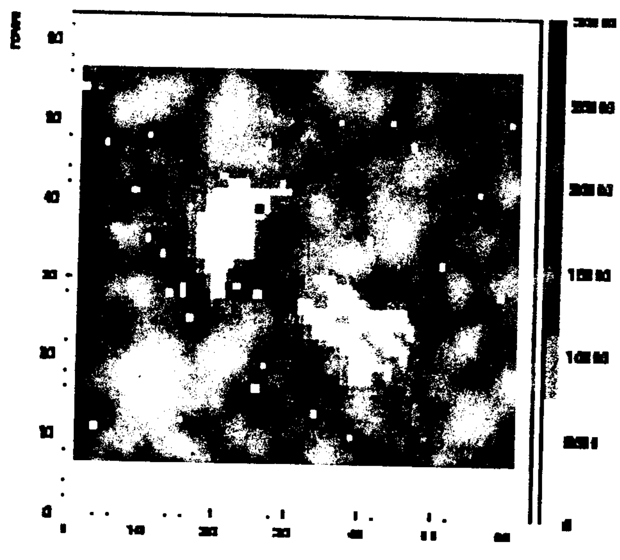
EFFECT FLAT FIELD CORRECTION

Compensation for inhomogeneity :

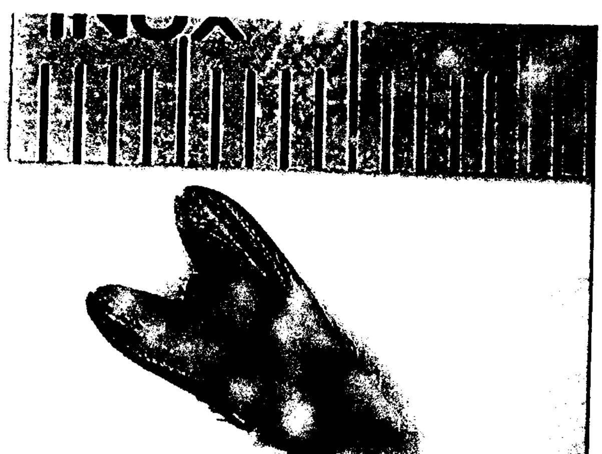
source geometry

pixel size, window absorption, etc





5.9 keV : SOURCE ^{55}Fe

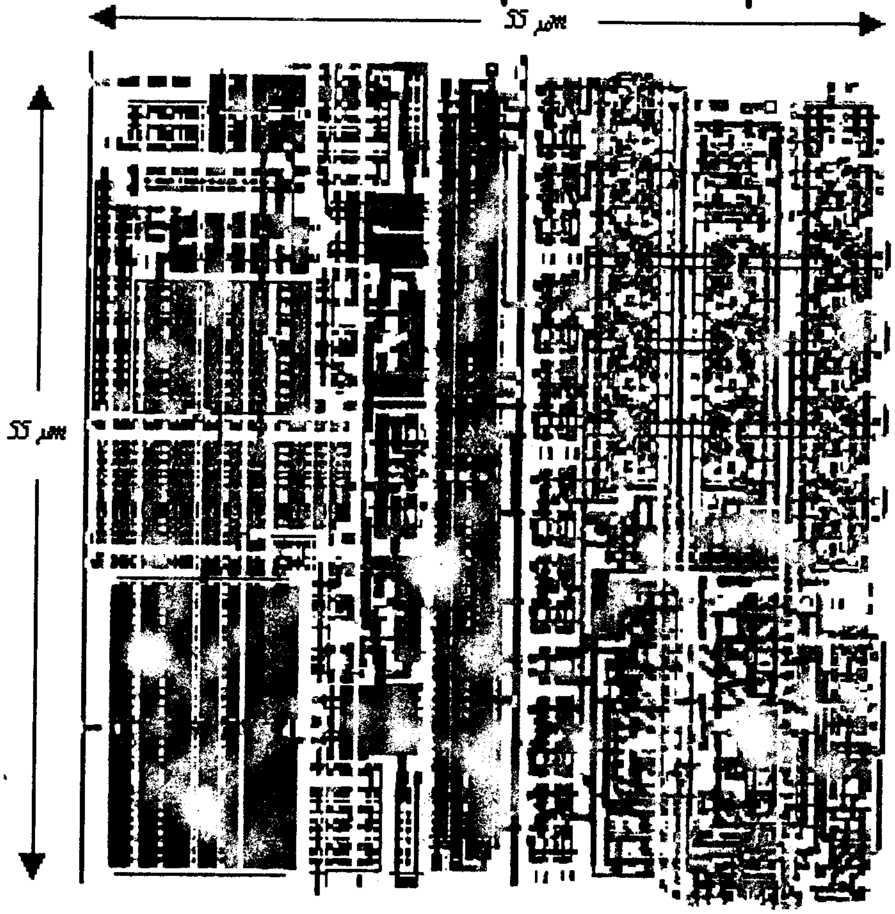


low energy improves contrast

Photon Counting Chip CERN

Medipix Collaboration

CELL PCC2 55μm x 55μm



+ and - polarity   0.25 μm CMOS

dark current compensation per pixel

window discriminator

linear range 80 000 e^-

13 bit counter + overflow

count rate ~ 10^{11} cm^{-2}

SYNCHROTRON DETECTORS

ANALOG INTEGRATION
SINGLE QUANTA
ADC IN PIXEL

BINARY COUNTING
MULTIPLE THRESHOLDS

MHz COUNTING IN PIXEL
10^{11} cm^{-2}

TIME RESOLUTION
FAST READOUT

CONTIGUOUS TILING

ASSEMBLY without DEAD AREA
EDGE TECHNOLOGY NEEDED

ASSEMBLY TECHNOLOGY

c.2. *Flip chip technology*

A flip-chip redistribution technique has been derived from the multilayer thin-film technology developed for high-density MCM interconnects (C22, C390). The technique uses Ni/Au plated copper conductors for redistribution. Benzo cyclo butene (BCB) polymer layers are used as isolation and solder mask layer. Solder bumps are realized by screen printing solder paste, reflow of the solder paste and wafer cleaning (flux removal). A schematic cross-section and picture of a redistributed die are shown in *figure 81*.

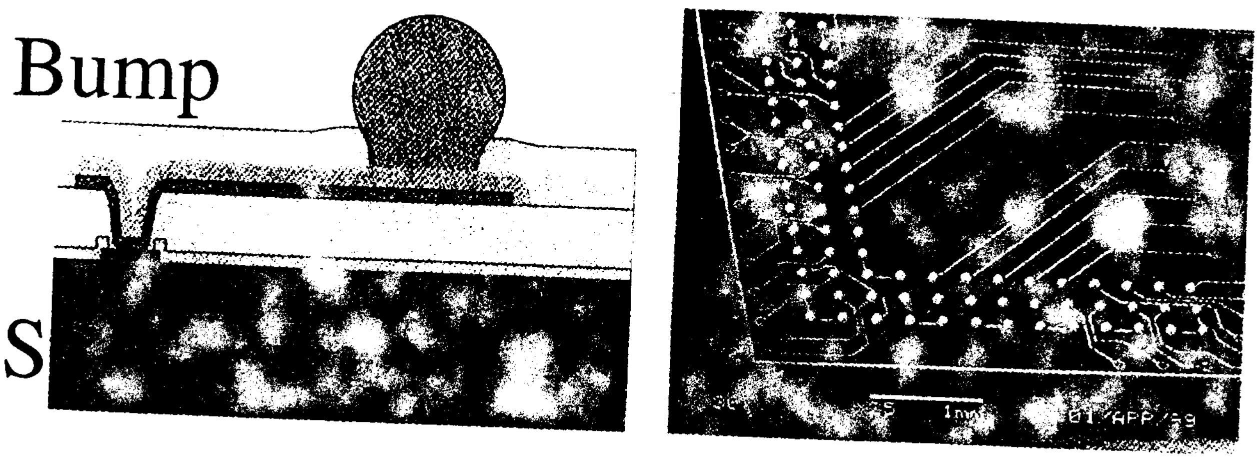


Figure 81: Schematic flip-chip redistribution technique (left) and SEM picture of a redistributed IC (right).

FLIP-CHIP BUMP CONTACT REDISTRIBUTION via MULTI-LAYER STRUCTURE

5 Cu / BCB (Benzo Cyclo Butene)

How Far Can One Go ? several mm ?

CONCLUSION

CHIP TECHNOLOGY -> NEW DETS

SINGLE QUANTUM PROCESSING

MHz COUNTING IN PIXEL

10^{11} cm^{-2}

FAST PROCESSES RESOLVABLE

CREATE DESIGN KNOW - HOW

CONTENTS

TRACKING PIXEL DETECTORS

COMPLEXITY inside PIXEL

PHOTON COUNTING PIXELS

SPECIFIC NEEDS SYNCHROTRON